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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.

EXAMINER	
ART UNIT	PAPER
	20060627

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

Notice of Allowability	Application No.	Applicant(s)	
	10/695,997	HATAKEYAMA, TSUTOMU	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *4/27/2006*.

2. ☒ The allowed claim(s) is/are *1-19*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 10/30/2003
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Response to Amendment

1. The corrected Figure 3 has been considered and is now in compliance with 37 CFR 1.121(d).

2. The amendments made to Claims 4, 11, and 17 to overcome 35 U.S.C. 112 rejections have been considered and the rejections are withdrawn.

3. The amendments to Claims 1, 3-8, 10-14, and 16-19 have been acknowledged.

4. Upon further Examiner Amendments, the Claims 1-19 will be in condition for allowance.

EXAMINER'S AMENDMENT

5. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

6. Authorization for this examiner's amendment was given in a telephone interview with Eckhard Kuesters (No. 28, 870) on 7/20/2006.

7. The following are Claims 1-19 as they should appear in amended form:

Claim 1 (Currently Amended): A cache memory, comprising: a data storage device ~~capable of storing~~ configured to store data which requires consistency of data with a main memory; and a storage controller which controls to store storing data which does not require consistency of data with said main memory, in an arbitrary data region in said data storage device, the arbitrary data region having an address space different from that of said main memory.

Claim 2 (Original): The cache memory according to claim 1, wherein said arbitrary data region is a data region designated by a programmer.

Claim 3 (Currently Amended): The cache memory according to claim 1, further comprising: a region designating unit which specifies addresses of said arbitrary data

region ~~for storing~~ configured to store data which does not require consistency of data with said main memory; and an address coincidence determination unit which determines whether ~~or not the designated~~ a particular address coincides with the addresses designated by said region ~~designated~~ designating unit.

Claim 4 (Currently Amended): The cache memory according to claim 3, further comprising a tag unit which stores addresses of data stored in said data storage device, wherein said data storage device and said tag unit ~~are composed of~~ include a plurality of ways including a plurality of indexes, respectively; and said region ~~designated~~ designating unit specifies whether ~~or not~~ data which does notrequire consistency of data with said main memory is stored in [[the]] a corresponding data region unit ~~is a unit of one way~~ for each way.

Claim 5 (Currently Amended): The cache memory according to claim 4, further comprising: a refill information storage which stores refill history information of refill in said data storage device; and a refill object selector which selects ways to be refilled based on the refill history information stored in said refill information storage and addresses designated by said region designating unit.

Claim 6 (Currently Amended): The cache memory according to claim 5, wherein said region ~~designated~~ designating unit includes: an address setting unit provided for each way, which sets addresses of data region for storing data which does not require consistency of data with said main memory; and a setting information storage provided for each way, which stores flag information indicative of whether ~~or not~~ a prescribed address is set to said address setting unit, wherein said refill object selector selects the way to be refilled based on the refill history information and the flag information.

Claim 7 (Currently Amended): The cache memory according to claim 1, wherein a look-aside type connection ~~method~~ configuration in which said main memory and said cache memory are connected to a common system bus, and a write-through writing ~~method~~ configuration in which data is written to said main memory and said cache memory at the same time are adopted.

Claim 8 (Currently Amended): A processor which adopts a look-aside type connection ~~method~~ configuration in which a main memory and a cache memory are connected to a common system bus, and a write-through writing ~~method~~ configuration in which data is written to said main memory and said cache memory at the same time, wherein said cache memory includes: a data storage device capable of storing data which requires consistency of data with said main memory; and a storage controller which controls ~~to store~~ storing data which does not require consistency of data with said main memory, in an arbitrary data region in said data storage device, the arbitrary data region having an address space different from that of said main memory.

Claim 9 (Original): The processor according to claim 8, wherein said arbitrary data region is a data region designated by a programmer.

Claim 10 (Currently Amended): The processor according to claim 8, further comprising: a region ~~designated~~ designating unit which specifies addresses of said arbitrary data region configured to store data which does not require consistency of data with said main memory; and an address coincidence determination unit which determines whether ~~or not the designated~~ a particular address coincides with the ~~address~~ addresses designated by said region ~~designated~~ designating unit.

Claim 11 (Currently Amended): The processor according to claim 10, further comprising a tag unit which stores addresses of data stored in said data storage device,wherein said data storage device and said tag unit ~~are composed of~~ include a plurality of ways including a plurality of indexes, respectively; and said region ~~designated~~ designating unit specifies whether ~~or not~~ data which does not require consistency of data with said main memory is stored in [[the]] a corresponding data region ~~is a unit of one way~~ for each way.

Claim 12 (Currently Amended): The processor according to claim 11, further comprising: a refill information storage which stores history information of refill in said data storage device; and a refill object selector which selects ways to be refilled based on the refill history information stored in said refill information storage and addresses designated by said region designating unit.

Claim 13 (Currently Amended): The processor according to claim 12, wherein region ~~designated~~ designating unit includes: an address setting unit provided for each way, which sets addresses of data region for storing data which does not require consistency of data with said main memory; and a setting information storage provided for each way, which stores flag information indicative of whether ~~or not~~ a prescribed address is set to said address setting unit, wherein said refill object selector selects the way to be refilled based on the refill history information and the flag information.

Claim 14 (Currently Amended): A cache control method which adopts a look-aside type connection method in which a main memory and a cache memory are connected to a common system bus, and a write-through writing method in which data is written into said main memory and said cache memory at the same time, comprising controlling ~~to store~~ storage of data which does not require consistency of data with said main memory in an arbitrary data region in a data storage device ~~to store data which does not require consistency of data said main memory~~, the arbitrary data region having an address space different from that of said main memory.

Claim 15 (Original): The cache control method according to claim 14, wherein said arbitrary data region is a data region designated by a programmer.

Claim 16 (Currently Amended): The cache control method according to claim 14, further comprising: designating, in advance addresses of said data region to store data which does not require consistency of data with said main memory; and determining whether ~~or not required~~ a particular address coincides with the designated address.

Claim 17 (Currently Amended): The cache control method according to claim 16, wherein said data storage device and a tag unit which stores addresses of data stored in said data storage device ~~are composed of~~ include a plurality of ways including a plurality of indexes; and it is designated whether ~~or not~~ data which does not require consistency of data with said main memory is stored in [[the]] a corresponding data region unit ~~in unit of one way~~ for each way.

Claim 18 (Currently Amended): The cache control method according to claim 17, further comprising: storing refill history information of refill in said data storage device; and selecting the way to be refilled based on the stored history information and the ~~address~~ addresses designated by said region ~~designate~~ designating unit.

Claim 19 (Currently Amended): The cache control method according to claim 18, comprising: setting addresses of a data region to store data which does not require consistency of data with said main memory for each way; storing the flag information indicative of whether ~~or not~~ addresses are set for each way; and selecting the way to be refilled based on said refill history information and said flag information.

Allowable Subject Matter

8. Claims 1-19 are allowed.

9. The following is an examiner's statement of reasons for allowance: Clams 1, 8, and 14 are three independent claims that differ only in their preambles, as Claim 1 references a "memory", Claim 8 references a "processor", and Claim 14 references a "method". The discussion of the reasons for allowance shall be directed to Claim 1, which the Examiner shall designate as the primary invention in this application. However, the reasons for allowance will also apply to Claims 8 and 14.

10. The allowability of Claim 1 will be described in detail. Claim 1 has a few separate parts that are not patentable if presented individually. However, the combination of the elements in Claim 1 allows for a novel invention that cannot be overcome by prior art. Specifically, Claim 1

denotes a cache memory that has a data storage device that is configured to store data that requires consistency of data with main memory. Furthermore, there is a storage controller that does not require consistency of data with the main memory, which is located in a region separate from the main memory. All of the underlined items above are the aspects of the invention that contribute to its originality. Since the cache memory has storage that is required to have consistency of data with the main memory, the scope of the invention becomes very limited. Furthermore, the storage controller that does not possess consistency of data (and is located separately from main memory) also adds to the invention's originality when combined with the first aspects of the Claim. Therefore, Claim 1 cannot be overcome by prior art and is patentable.

11. Dependent Claims 2-7, 9-13, and 15-19 are all in condition for allowance due to the allowability of Claims 1, 8, and 14 respectively.

12. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on M-Th from 8AM-6PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lev Iwashko

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100